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Design of Error-Tolerant CMOS Adder Using optimized Transistor Count

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Abstract: In modern VLSI technology, the occurrence of all kinds of errors cannot be avoided. So, the error-tolerant adder (ETA) is designed. Error-tolerant circuit may produce erroneous outputs but the motivation for using it is an increase in effective yield, improved revenues, and lower-cost parts. It can be seen as a new trade-off parameter besides power and speed. The three important considerations of VLSI design is power, area, and delay. Number of transistors used in adder also plays an important role in area. The proposed design of Error tolerant adder, transistor count has been reduced by incorporating the 4 transistor XOR gate in the design of Adder. When compared to other ETAs, the proposed optimized ETA is able to achieve nearly 50% improvement in the area (transistor count) with considerable power.

Keywords: VLSI, Error-Tolerant Adder (ETA), Error Tolerance (ET), Power-Delay Product (PDP).

I. INTRODUCTION

In conventional digital VLSI design, usually it is assumed that a usable circuit/system should always provide definite and accurate results. But in fact, such perfect operations are seldom needed in our non digital worldly experiences. The world accepts "analog computation," which generates "good enough" results rather than totally accurate results [1]. Human senses for example do not require everything to be exact. Furthermore due to the advances in transistor size scaling, factors such as noise and process variations which are previously insignificant are becoming important in today's digital IC design. If we can tolerate these erroneous results, tremendous improvements in both the power consumption and speed performance will be achieved.

So, the concept of Error tolerance is used in such circuits. If the application can accept some errors, i.e. the application is Error- tolerant (ET), a large reduction in power and an increased in speed can be simultaneously achieved. Any circuit is called error tolerant if: It contains defects that cause internal and may cause external errors and the system that incorporates this circuit produces acceptable results [2]. With increased size of data sets and the need for quick response there is requirement of adder which is large and fast. The traditional ripple-carry adder (RCA) is therefore no longer suitable for large adders because of its low-speed performance. Many different types of fast adders, such as the carry-skip adder (CSK) [3], carry-select adder (CSL) [4], and carry-look-ahead adder (CLA) [5], have been developed. However, there are always trade-offs between speed and power and area. So, by sacrificing some accuracy, the ETA can attain great improvement in both the power consumption and speed performance and hence is a potential solution to this problem.

There are various proposed designs of error tolerant adder but all the types of error tolerant adder have their own advantages and disadvantages in term of power, delay and size which are of main consideration factors in VLSI. Some of the types of Error tolerant adder have large power consumption and some have more delay, but all types of ETA have been designed using large number of transistor as in all the adder conventional 28 transistor full adder has been used.

So in the proposed design of new error tolerant adder, basic type of error tolerant adder ETAI is optimized by using lesser transistor in the circuit. Different reduced transistor full adders [6, 7] are designed but in the proposed design of optimized ETAI, 14 transistors full adder [8] is used as compared to conventional 28 transistor full adder. Hence in the optimized ETAI, better results in terms of power, delay and size can be achieved.

II. ERROR-TOLERANT ADDER DESIGNS

The proposed design of error tolerant adder modifies the existing ETAI in terms of size by reducing the transistor count in the Circuit. The first error –tolerant adder designed was ETA I [9]. This novel type of adder trades certain amount of accuracy for significant power saving and performance improvement. In this adder input operand is split into two parts: an accurate part that includes several higher order bits and the inaccurate part that is made up of the remaining lower order bits. The addition process starts from the middle (joining point of the two parts) toward the two opposite directions simultaneously.

The addition of the higher order bits (accurate part) of the input operands is performed from right to left (LSB to MSB) and normal addition method is applied. The lower order bits of the input operands (inaccurate part) required special addition mechanism. No carry signal will be generated or taken in at any bit position to eliminate the carry propagation path in the inaccurate part of the error tolerant adder I.

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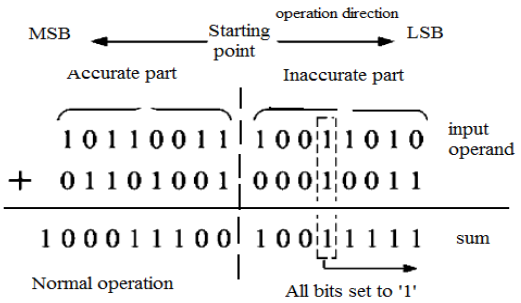

Fig. 1 Addition arithmetic in ETA I [9]

To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted in which every bit position from left to right (MSB to LSB) is checked and if both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position but if both input bits are "1," the checking process stopped and from this bit onward, all sum bits to the right are set to "1." Extensive comparisons with conventional digital adders showed that the proposed ETA-I outperformed the conventional adders in both power consumption and speed performance. But this adder has problem of adding small number inputs.

Second type of Error-tolerant adder is ETA II [10]. It achieves 60% improvement in power delay product. Different from ETAI, ETAII does not eliminate the entire or part of the carry propagation path. Instead, it splits the entire carry propagation path into a number of short paths and completes the carry propagations in these short paths concurrently. In this way, the speed performance of the adder can be significantly improved and with almost no degradation in its power consumption. Architecture of ETAII depicted that for an N-bit adder, it is divided into M($M \geq 2$) blocks. Each block contains N/M bits and is consists of two separate circuitries – Carry generator and Sum generator. The Carry generator creates the carry-out signal. It does not take in carry signal from previous block. The Sum generator however, takes the carry-in signal from previous block to generate its sum output bits.

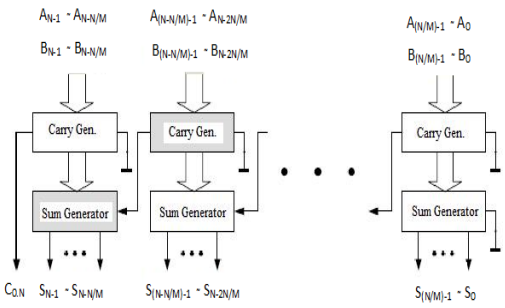

Fig. 2 Block diagram of ETA II [10]

But ETAII has a problem of degraded accuracy for large operands, which was removed by ETA IIM proposed by author in same paper. In ETAIIM, the higher order bits were kept more accurate than the lower order bits as they play a more important role in representing a number. Therefore, for the higher order bit positions, more input bits should be considered when calculating the carry signals. In this structure, the first three carry generators are cascaded together to generate the carry signals for the two highest blocks. In this way, the carry signal for the highest block is generated by the preceding 12 bits and the carry signal for the second block is generated by the preceding 8 bits and so on.

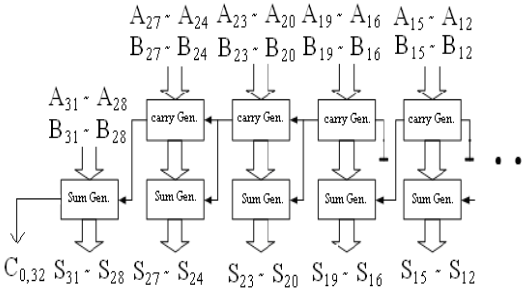

Fig.3 Structure of modified ETA IIM [10]

Third type of error –tolerant adder is ETAIII [11]. ETAIII is able to eradicate the unavoidable performance trade-off on delay and accuracy faced by ETAI and other digital circuits. In this adder division of input operand into accurate and inaccurate part is not predetermined. Instead a circuit called Selector is designed to determine the number of bits to be divided among accurate and inaccurate part. Depending on the input operand, this selector circuit Divide accurate and inaccurate parts. If input operand is small more number of bits are assigned to accurate part to get accurate results and if number is large less number of bits are assigned to accurate part to speed up the operation. As depicted in fig. 4, ETAIII involves two types of adders, Full adders (FA) and Speed adders (SA). FA is conventional full adder and SA is similar to adder used in the inaccurate part of ETAI.

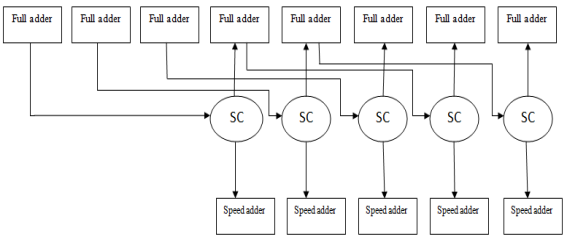

Fig. 4 Block diagram of ETA III[11]

Next and the latest type of Error-tolerant adder designed was ETAIV [12]. ETAIV is able to eradicate the unavoidable performance trade-off on delay and accuracy faced by ETAII and other digital circuits. In this adder more number of bits are used to calculate the Carry bit in order to improve the accuracy. ETAIV is derived from Carry Select Adder (CSL). The difference between ETAIV and CSA is that a 2-to-1 multiplexer (MUX2) is deployed to break the carry chain into two stages. Two Carry Generators, Type I and II, are also engaged in the circuit. And as illustrated in Fig. 6, an N-bit adder is divided into N/X blocks (each Sum Generator block has X bits). In the actual design however, N may not be exactly divisible by X. Both Carry Generator Type I and II have

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the same X bits and perform their functions simultaneously, calculating the carry outputs with X bits accuracy.

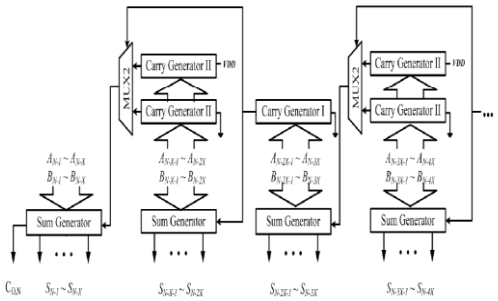


Fig. 6 Block diagram of ETA IV [12]

III. PROPOSED ERROR TOLERANT ADDER

The addition arithmetic used in optimized ETAI is same as ETAI, the input operands is divided into two parts: an accurate part that includes several higher order bits and the inaccurate part that is made up of the remaining lower order bits. The addition process starts from the middle (joining point of the two parts) toward the two opposite directions simultaneously. The addition of the bits in accurate part is performed as normal addition method and bits of inaccurate part required special addition mechanism. No carry signal will be generated or taken in at any bit position to eliminate the carry propagation path. To minimize the overall error due to the elimination of the carry chain, a special strategy is adapted, and can be described as follow: 1) check every bit position from left to right (MSB to LSB); 2) if both input bits are "0" or different, normal one-bit addition is performed and the operation proceeds to next bit position; 3) if both input bits are "1," the checking process stopped and from this bit onward, all sum bits to the right are set to "1."

The block diagram of the hardware implementation of optimized ETAI consists of two parts: an accurate part and an inaccurate part. The accurate part is constructed using a 14 transistor full and the carry-in of this adder is connected to ground. The inaccurate part constitutes two blocks: a carry-free seed adder block and a control block. The control block is used to generate the control signals, to determine the working mode of the carry-free speed adder block. In this design of optimized ETAI, we have divided the 32-bit adder by putting 12 bits in the accurate part and 20 bits in the inaccurate part.

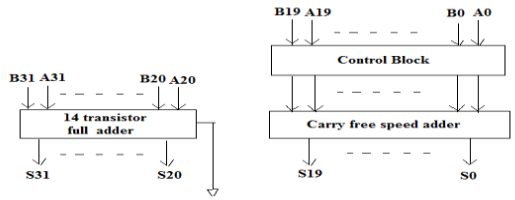


Fig.7 Hardware circuit of the proposed Optimized ETAI

In this proposed work of 32-bit Error Tolerant Adder, the accurate part has 12 bits. So here 14 transistor full adder is used as compared to conventional 28 transistor full adder. Hence, transistor count is reduced by 50% in the accurate part of error tolerant adder. The 14 transistor full adder provides better results in terms of power and delay. Circuit Diagram for 14 transistor full adder is shown in fig 8.

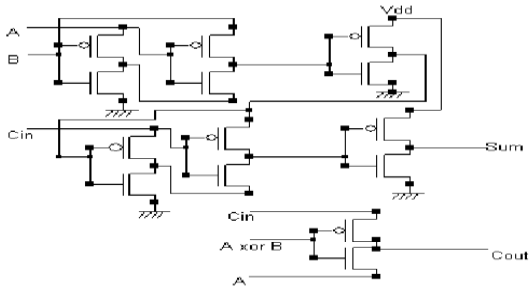


Fig. 8 14 transistor full adder [8]

In this accurate part, 12 full adders are cascaded using Ripple carry adder method to provide the most significant bits of the sum output of optimized ETAI. The Schematic for accurate part of optimized ETAI is shown in fig. 9.

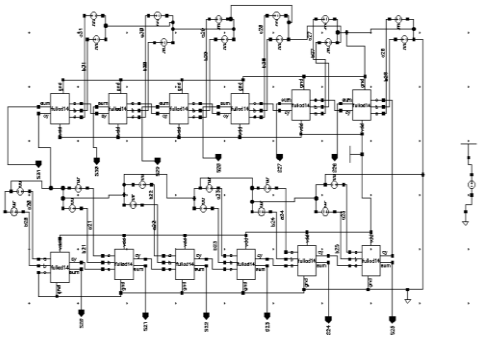
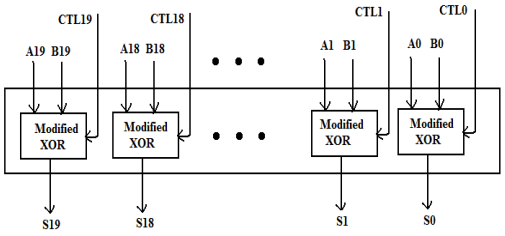
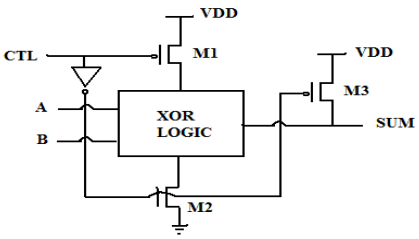


Fig 9 Schematic for accurate part of optimized ETAI

The inaccurate part is the most critical section in this ETA as it determines the accuracy, speed performance, and power consumption of the adder. The inaccurate part consists of two blocks: the carry free speed adder block and the control block. The carry-free speed adder block is made up of 20 modified XOR gates, and each of which is used to generate a sum bit. The circuit diagram of the modified XOR gate using 6 transistor XOR gate is presented in Fig.10.



(a)



(b)

Fig.10 Carry free speed adder (a) Overall architecture (b) Schematic for modified XOR gate [9]

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The Schematic for carry free speed adder block is as shown in fig. 11.

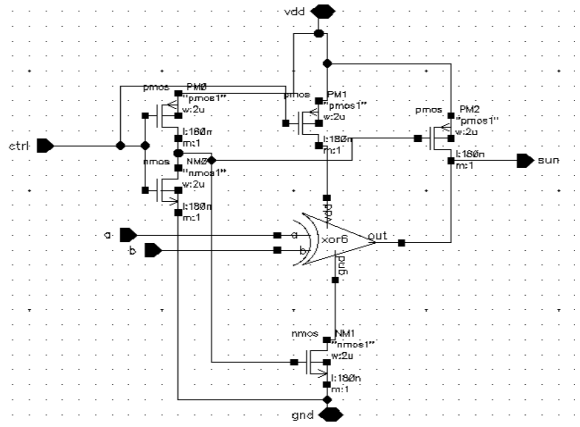

Fig 11 Schematic for Carry free speed adder block

The control block in the inaccurate part is made up of 20 control signal generating cells (CSGCs) and each cell generates a control signal for the modified XOR gate at the corresponding bit position in the carry-free speed adder block. Two types of CSGC, labelled as control1 and control2 are designed and shown in fig 12. The control signal generated by the leftmost cell of each group is connected to the input of the leftmost cell in next group. The extra connections allow the propagated high control signal to "jump" from one group to another instead of passing through all the 20 cells. Hence, the worst case propagation consists of only 11 cells.

(a) (b)

Fig. 12 (a) Control1 block (b) Control2 block [9]

Instead of a long chain of 20 cascaded CSGCs, the control block is arranged into four equal-sized groups, with additional connections between every two neighbouring groups. The overall architecture for Cascaded CSGCs is shown below in fig. 13.

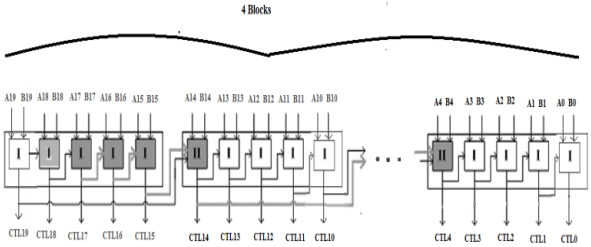

Fig.13 Overall architecture of CSGCs

So the inaccurate part of optimized error tolerant adder is designed using the carry free speed adder and control blocks. Same as control signal generating cell, inaccurate part is arranged into four equal sized groups. Each group consist of five control blocks and five carry free speed adder. The Schematic for inaccurate ETAI is shown in fig. 14.

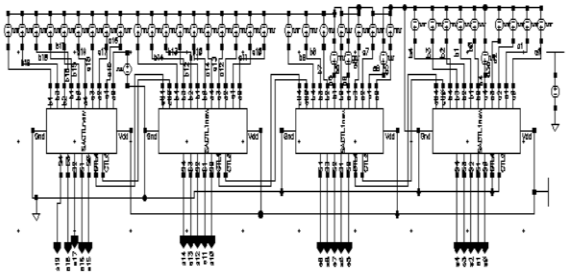

Fig.14 Schematic for inaccurate Optimized ETA

IV. RESULTS AND DISCUSSIONS

The Schematic of proposed design has been developed using Cadence Virtuoso Schematic Editor and simulated with Cadence Virtuoso Analog Design Environment. All the circuits were implemented using cadence virtuoso 180nm technology. The results show that the power utilization in case of proposed design is very less as compared to that previous design of Error tolerant adder and delay is also comparable to other designs with decreased transistor count which future reduce the size. The output waveform for accurate part of optimized ETAI is shown in fig. 15.

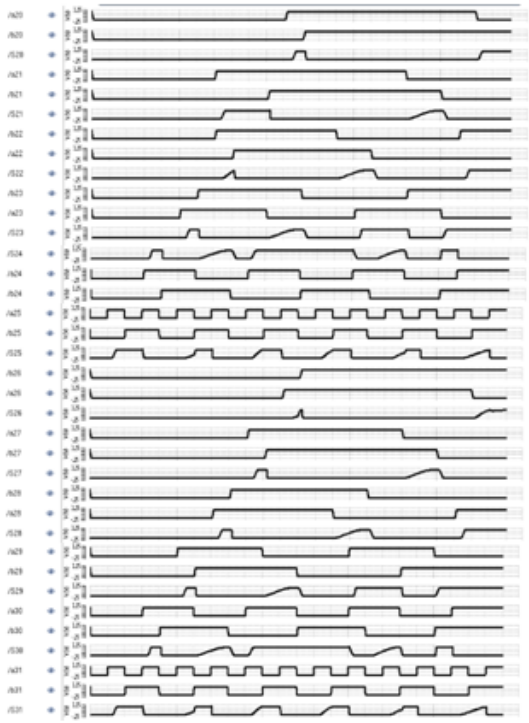

Fig.15 Output waveform of Accurate part of optimized ETAI

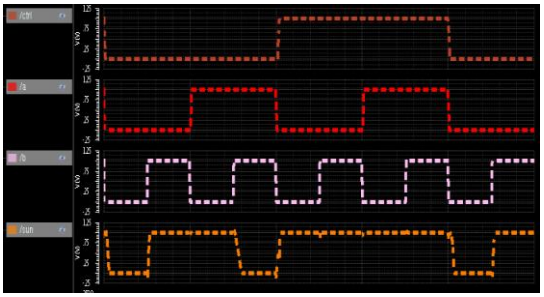

Fig.16 Output waveform for carry free speed adder block

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The output waveform for carry free speed adder block after simulation is shown in fig.16 and the output for 10 MSB bits for inaccurate part of optimized ETAI is shown in fig.17.

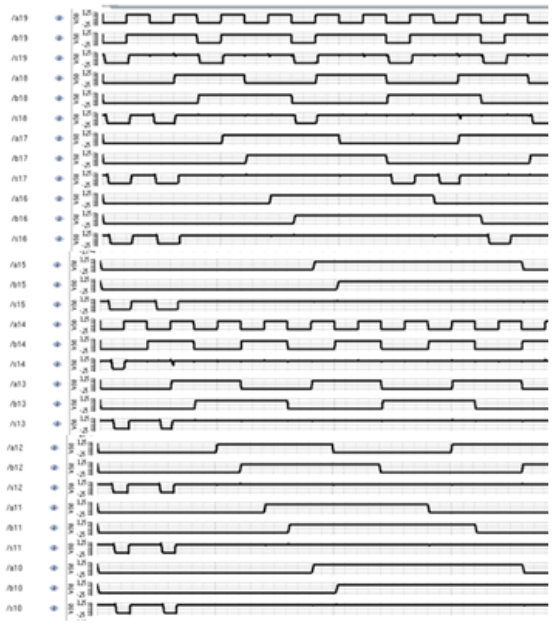

Fig.17 Output of inaccurate part of optimized ETAI for 10MSB bits

TABLE I

Simulation result for optimized ETA versus speed adders and other ETAs.

Parameter	ETAI [9]	ETAII [10]	ETAII M [10]	ETAIII [11]	ETAIV [12]	Proposed ETA
Power (mW)	0.13	0.24	0.24	0.18	0.25	0.22
Delay (ns)	2.29	0.85	1.39	2.20	1.03	10.5
Transistor Count	1006	1372	1372	1622	1444	628

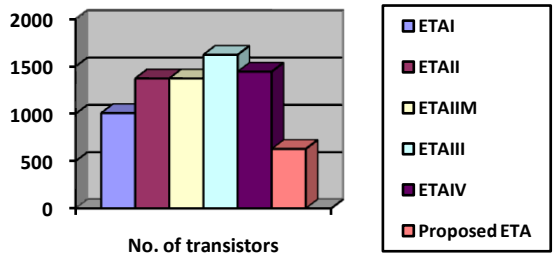

Fig. 18 Comparison of various ETAs with proposed ETA based on transistor count

As seen from the simulation results, the proposed ETA use very transistors as compared to all other ETAs and have comparable Power. In this sense, optimized ETA offers an overall better performance for error tolerant applications where area is of main concern as it uses very less number of transistors. This low-power and less area optimized ETA is to greater extend competitive than the conventional adders and other ETAs, especially in the low accuracy and space applications. One example of such applications is in DSP, for portable devices such as cell phones and laptops.

IV. CONCLUSION AND FUTURE SCOPE

The 'Optimized error tolerant adder' was thus designed with an idea to minimize the delay and power consumption with reduced size using optimized transistor count. Simulation results shows that the proposed optimized ETA is able to achieve nearly 50% improvement in area (transistor Count) as compared to other ETAs. If accuracy and transistor count is reduced than power and delay will be affected or vice versa. With decrease in transistor count, delay has been increased in this design. In future, work can be done to reduce delay factors in this design, while considering accuracy to desired level and keeping power as low as possible with decrease in the transistor count.

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